OVUV\_OTUT\_CMP

Revision History

|  |  |  |  |
| --- | --- | --- | --- |
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# OVUV\_OTUT\_CMP

## Introduction

The OVUV\_OTUT\_CMP is a 31-channel comparator. The comparator can generate fault warning signal when the chip is over-voltage, under-voltage, over-temperature, and under-temperature. Thus, it can be applied to protect the chip from entering into abnormal working state.

The OVUV\_OTUT\_CMP module has the following features:

• Latch OVUV\_OTUT\_EN\_REG, CELL\_OV\_THRESH\_REG, CELL\_UV\_THRESH\_REG, GPIO\_OTUT\_THRESH\_SEL\_REG, GPIO\_OT\_PACK\_THRESH\_REG, GPIO\_OT\_PCB\_THRESH\_REG, GPIO\_UT\_PACK\_THRESH\_REG, GPIO\_UT\_PCB\_THRESH\_REG, CB\_OT\_PACK\_THRESH\_REG, CB\_OT\_PCB\_THRESH\_REG, OVUV\_DEGL\_REG to OVUV\_OTUT\_EN, CELL\_OV\_THRESH, CELL\_UV\_THRESH, GPIO\_OTUT\_THRESH\_SEL, GPIO\_OT\_PACK\_THRESH, GPIO\_OT\_PCB\_THRESH, GPIO\_UT\_PACK\_THRESH, GPIO\_UT\_PCB\_THRESH, CB\_OT\_PACK\_THRESH, CB\_OT\_PCB\_THRESH, OVUV\_DEGL once MON\_WAKE\_GO or ADC\_GO\_DLY is high; (HWR001\_OVUV\_OTUT\_CMP)

• Compare ADC\_DATA\_LPF with CELL\_OV\_THRESH and CELL\_UV\_THRESH when RR\_END is high, and output CELL\_OVUV according to OVUV\_DEGL when OVUV\_OTUT\_EN is high; (HWR002\_OVUV\_OTUT\_CMP)

• Compare OTH\_ADC\_DATA with GPIO\_OT\_PACK\_THRESH, GPIO\_OT\_PCB\_THRESH, GPIO\_UT\_PACK\_THRESH, GPIO\_UT\_PCB\_THRESH, CB\_OT\_PACK\_THRESH, CB\_OT\_PCB\_THRESH according to GPIO\_OTUT\_THRESH\_SEL when RR\_END is high, and output GPIO\_OTUT, GPIO\_CBOT when OVUV\_OTUT\_EN is high; (HWR003\_OVUV\_OTUT\_CMP)

• Reset when OVUV\_OTUT\_EN is low; (HWR004\_OVUV\_OTUT\_CMP)

• Output CELL\_OVUV until counter=OVUV\_DEGL; (HWR005\_OVUV\_OTUT\_CMP)

• The counter will +1 when fault is detected; (HWR005\_OVUV\_OTUT\_CMP)

• The max of counter is OVUV\_DEGL; (HWR005\_OVUV\_OTUT\_CMP)

• The counter will -1 when fault is not detected; (HWR005\_OVUV\_OTUT\_CMP)

• Update TWARN\_THRESH\_REG into TWARN\_THRESH when ADC\_GO\_DLY or MON\_WAKE\_GO is high; (HWSR1\_OVUV\_OTUT\_CMP)

• Compare the gap between OTH\_ADC\_DATA with TWARN\_THRESH when RR\_END is high; (Once over range, output TWARN) (HWSR2\_OVUV\_OTUT\_CMP)

• TWARN TWARN\_THRESH covers from 110℃ to 145℃, 5℃ step; (HWSR2\_OVUV\_OTUT\_CMP)

• OVUV\_OTUT\_EN is ignored when TWARN comparison. (HWSR3\_OVUV\_OTUT\_CMP)

## Register Definition

### Register Map

Table 1 OVUV\_OTUT\_CMP Register Map

|  |  |  |  |
| --- | --- | --- | --- |
| **ADDRESS** | **NAME** | **DESCRIPTION** | **RESET VALUE** |
| **OVUV\_OTUT\_CMP** | | | |
| 0x0000 | **OVUV\_OTUT \_CONF1** | OVUV\_OTUT\_CMP configuration register 1 | 0x80 |
| 0x0001 | **OVUV\_OTUT \_CONF2** | OVUV\_OTUT\_CMP configuration register 2 | 0x60 |
| 0x0002 | **OVUV\_OTUT \_CONF3** | OVUV\_OTUT\_CMP configuration register 3 | 0x60 |
| 0x0003 | **OVUV\_OTUT \_CONF4** | OVUV\_OTUT\_CMP configuration register 4 | 0x7E |
| 0x0004 | **OVUV\_OTUT \_CONF5** | OVUV\_OTUT\_CMP configuration register 5 | 0x7E |
| 0x0005 | **OVUV\_OTUT \_CONF6** | OVUV\_OTUT\_CMP configuration register 6 | 0x00 |
| 0x0006 | **OVUV\_OTUT \_CONF7** | OVUV\_OTUT\_CMP configuration register 7 | 0x00 |
| 0x0007 | **CB\_CONF1** | CB configuration register 1 | 0x7F |
| 0x0008 | **CB\_CONF2** | CB configuration register 2 | 0x78 |
| 0x000A | **TWARN\_CONF** | TWARN configuration register | 0x03 |
| 0x1FF6 | **ADC\_CTRL** | ADC control register | 0x00 |

### OVUV\_OTUT\_CONF1

Register 1. OVUV\_OTUT \_CONF1 (OVUV\_OTUT\_CMP configuration register 1, offset 0x0000)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **BIT** | **NAME** | **ACCESS** | **RESET** | **DESCRIPTION** |
| 7 | **OVUV\_OTUT\_EN** | R/W | 1’b1 | OVUV\_OTUT\_CMP Enable Bit  0: Disable  1: Enable |
| 6:5 | **REV** | R | 2’b00 | Reserved |
| 4:0 | **OVUV\_ DEGL** | R/W | 5’h00 | OVUV\_OTUT\_CMP Deglitch Number  0 0000:1  0 0001:2  0 0010:3  ...  1 1111:32 |

### OVUV\_OTUT\_CONF2

Register 2. OVUV\_OTUT \_CONF2 (OVUV\_OTUT\_CMP configuration register 2, offset 0x0001)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **BIT** | **NAME** | **ACCESS** | **RESET** | **DESCRIPTION** |
| 7 | **REV** | R | 1’b0 | Reserved |
| 6:0 | **OV\_THR** | R/W | 7’h60 | Over-voltage Threshold  000 0000:2V  000 0001:2.025V  000 0010:2.05V  ...  111 0111:4.975V  111 1000-111 1111:5V |

### OVUV\_OTUT\_CONF3

Register 3. OVUV\_OTUT \_CONF3 (OVUV\_OTUT\_CMP configuration register 3, offset 0x0002)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **BIT** | **NAME** | **ACCESS** | **RESET** | **DESCRIPTION** |
| 7 | **REV** | R | 1’b0 | Reserved |
| 6:0 | **UV\_THR** | R/W | 7’h60 | Under-voltage Threshold  000 0000:0.7V  000 0001:0.725V  000 0010:0.75V  ...  111 1111:3.875V |

### OVUV\_OTUT\_CONF4

Register 4. OVUV\_OTUT \_CONF4 (OVUV\_OTUT\_CMP configuration register 4, offset 0x0003)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **BIT** | **NAME** | **ACCESS** | **RESET** | **DESCRIPTION** |
| 7:3 | **OT\_ PACK\_THR** | R/W | 1’h0F | Over-temperature Threshold (PACK)  0 0000:5%  0 0001:6%  ...  1 1111:36% |
| 2:0 | **UT\_ PACK\_THR** | R/W | 3’h6 | Under-temperature Threshold (PACK)  000:76%  001:78%  ...  111:90% |

### OVUV\_OTUT\_CONF5

Register 5. OVUV\_OTUT \_CONF5 (OVUV\_OTUT\_CMP configuration register 5, offset 0x0004)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **BIT** | **NAME** | **ACCESS** | **RESET** | **DESCRIPTION** |
| 7:3 | **OT\_ PCB\_THR** | R/W | 1’h0F | Over-temperature Threshold (PCB)  0 0000:5%  0 0001:6%  ...  1 1111:36% |
| 2:0 | **UT\_ PCB\_THR** | R/W | 3’h6 | Under-temperature Threshold (PCB)  000:76%  001:78%  ...  111:90% |

### OVUV\_OTUT\_CONF6

Register 6. OVUV\_OTUT \_CONF6 (OVUV\_OTUT\_CMP configuration register 6, offset 0x0005)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **BIT** | **NAME** | **ACCESS** | **RESET** | **DESCRIPTION** |
| 7 | **GPIO7\_THR\_SEL** | R/W | 1’b0 | GPIO7 Threshold Select Bit  0: PACK  1: PCB |
| 6 | **GPIO6\_THR\_SEL** | R/W | 1’b0 | GPIO6 Threshold Select Bit  0: PACK  1: PCB |
| 5 | **GPIO5\_THR\_SEL** | R/W | 1’b0 | GPIO5 Threshold Select Bit  0: PACK  1: PCB |
| 4 | **GPIO4\_THR\_SEL** | R/W | 1’b0 | GPIO4 Threshold Select Bit  0: PACK  1: PCB |
| 3 | **GPIO3\_THR\_SEL** | R/W | 1’b0 | GPIO3 Threshold Select Bit  0: PACK  1: PCB |
| 2 | **GPIO2\_THR\_SEL** | R/W | 1’b0 | GPIO2 Threshold Select Bit  0: PACK  1: PCB |
| 1 | **GPIO1\_THR\_SEL** | R/W | 1’b0 | GPIO1 Threshold Select Bit  0: PACK  1: PCB |
| 0 | **GPIO0\_THR\_SEL** | R/W | 1’b0 | GPIO0 Threshold Select Bit  0: PACK  1: PCB |

### OVUV\_OTUT\_CONF7

Register 7. OVUV\_OTUT \_CONF7 (OVUV\_OTUT\_CMP configuration register 7, offset 0x0006)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **BIT** | **NAME** | **ACCESS** | **RESET** | **DESCRIPTION** |
| 7:4 | **REV** | R | 4’h0 | Reserved |
| 3 | **GPIO11\_THR\_SEL** | R/W | 1’b0 | GPIO11 Threshold Select Bit  0: PACK  1: PCB |
| 2 | **GPIO10\_THR\_SEL** | R/W | 1’b0 | GPIO10 Threshold Select Bit  0: PACK  1: PCB |
| 1 | **GPIO9\_THR\_SEL** | R/W | 1’b0 | GPIO9 Threshold Select Bit  0: PACK  1: PCB |
| 0 | **GPIO8\_THR\_SEL** | R/W | 1’b0 | GPIO8 Threshold Select Bit  0: PACK  1: PCB |

### CB\_CONF1

Register 8. CB\_CONF1 (CB configuration register 1, offset 0x0007)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **BIT** | **NAME** | ACCESS | **RESET** | **DESCRIPTION** |
| 7:3 | **CB\_ROT\_PACK\_THR** | R/W | 5’h0F | CB Over-temperature Threshold (PACK)  0 0000: 5%  0 0001: 6%  ...  1 1111: 36% |
| 2:0 | **--** | -- | -- | -- |

### CB\_CONF2

Register 9. CB\_CONF2 (CB configuration register 2, offset 0x0008)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **BIT** | **NAME** | **ACCESS** | **RESET** | **DESCRIPTION** |
| 7:3 | **CB\_ROT\_PCB\_THR** | R/W | 5’h0F | CB Over-temperature Threshold (PCB)  0 0000: 5%  0 0001: 6%  ...  1 1111: 36% |
| 2:0 | **--** | -- | -- | -- |

### TWARN\_CONF

Register 10. TWARN\_CONF (TWARN configuration register, offset 0x000A)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **BIT** | **NAME** | **ACCESS** | **RESET** | **DESCRIPTION** |
| 7:3 | **REV** | R | 5’h00 | Reserved |
| 2:0 | **TWARN\_THR** | R/W | 3’h3 | TWARN Threshold  000:110℃  001:115℃  …  111:145℃ |

### ADC\_CTRL

Register 11. ADC\_CTRL (ADC control register, offset 0x1FF6)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **BIT** | **NAME** | **ACCESS** | **RESET** | **DESCRIPTION** |
| 7 | **MON\_WAKE\_GO** | R/W | 1’b0 | Mon-wake Starting Bit  0: Ready  1: Execute |
| 6:3 | **REV** | R | 4’h0 | Reserved |
| 2:0 | **--** | -- | -- | -- |

## Function Details

### Block Diagram

The main elements of OVUV\_OTUT\_CMP and their interactions are shown in Fig 1.



Fig 1. OVUV\_OTUT\_CMP Block Diagram

### OVUV\_OTUT\_CMP IO Descriptions

This section provides the OVUV\_OTUT\_CMP IO descriptions.

Table 2 OVUV\_OTUT\_CMP IO descriptions

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Signal** | **Width** | **Duration** | **I/O** | **Default Value** | **Register** |
| CLK\_SLOW\_SC | 1 | -- | I | -- | -- |
| resetb\_SR\_CLK\_SLOW | 1 | -- | I | -- | -- |
| ADC\_SGLE\_GO\_DLY | 1 | >1 CLK\_SLOW\_SC | I | -- | -- |
| ADC\_CNTI\_GO\_DLY | 1 | >1 CLK\_SLOW\_SC | I | -- | -- |
| MON\_WAKE\_GO | 1 | >1 CLK\_SLOW\_SC | I | -- | MON\_WAKE\_GO |
| OVUV\_OTUT\_EN\_REG | 1 | -- | I | -- | OVUV\_OTUT\_EN |
| CELL\_OV\_THRESH\_REG | 7 | -- | I | -- | OV\_THR |
| CELL\_UV\_THRESH\_REG | 7 | -- | I | -- | UV\_THR |
| GPIO\_OTUT\_THRESH\_SEL\_REG | 12 | -- | I | -- | OVUV\_OTUT \_CONF6  OVUV\_OTUT \_CONF7 |
| GPIO\_OT\_PACK\_THRESH\_REG | 5 | -- | I | -- | OT\_ PACK\_THR |
| GPIO\_OT\_PCB\_THRESH\_REG | 5 | -- | I | -- | OT\_ PCB\_THR |
| GPIO\_UT\_PACK\_THRESH\_REG | 3 | -- | I | -- | UT\_ PACK\_THR |
| GPIO\_UT\_PCB\_THRESH\_REG | 3 | -- | I | -- | UT\_ PCB\_THR |
| CB\_OT\_PACK\_THRESH\_REG | 5 | -- | I | -- | CB\_ROT\_PACK\_THR |
| CB\_OT\_PCB \_THRESH\_REG | 5 | -- | I | -- | CB\_ROT\_PCB\_THR |
| TWARN\_THRESH\_REG | 3 | -- | I | -- | TWARN\_THR |
| OVUV\_DEGL\_REG | 5 | -- | I | -- | OVUV\_ DEGL |
| ADC\_DATA\_LPF\_CH1—  ADC\_DATA\_LPF\_CH18 | 16 | -- | I | -- | -- |
| ADC\_DATA\_GPIO\_CH1—  ADC\_DATA\_GPIO\_CH12 | 16 | -- | I | -- | -- |
| ADC\_DATA\_VPTAT | 16 | -- | I | -- | -- |
| RR\_END | 1 | 16 CLK\_ADC\_SC | I | -- | -- |
| TWARN | 1 | -- | O | 1’b0 | -- |
| CELL\_OV | 18 | -- | O | 18’h00000 | -- |
| CELL\_UV | 18 | -- | O | 18’h00000 | -- |
| GPIO\_OT | 12 | -- | O | 12’h000 | -- |
| GPIO\_UT | 12 | -- | O | 12’h000 | -- |
| GPIO\_CBOT | 1 | -- | O | 1’b0 | -- |

### OVUV\_OTUT\_CMP Key Signal Descriptions

Table 3 OVUV\_OTUT\_CMP key signal descriptions

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal** | **Width** | **Duration** | **Default Value** | **Description** |
| OVUV\_OTUT\_CMP\_START | 1 | 2 CLK\_SLOW\_SC | 1’b0 | It represents starting comparing. |
| CMP\_UNDERWAY | 1 | -- | 1’b0 | The CMP\_UNDERWAY = 1 when the RR\_END\_SYNC\_POS (RR\_END after synchronization and rising edge detection) appear. It lasts for 31 clock periods. It represents the comparing is underway. And when CMP\_UNDERWAY = 1, the register value can not load in this module. |
| RELOAD\_START | 1 | 1 CLK\_SLOW\_SC | 1’b0 | When the rising edge of OVUV\_OTUT\_CMP\_START is detected, the RELOAD\_START = 1. And when the comparing is underway, the RELOAD\_START is hold, and when the comparing is not underway, the RELOAD\_START is cleared at the next clock edge. It is used to record the OVUV\_OTUT\_CMP\_START requirement, and after comparing ends, enable loading register. |
| RELOAD\_EN | 1 | 1 CLK\_SLOW\_SC | 1’b0 | It is generated by RELOAD\_START except the part of comparing being underway. It is used to enable loading register. |
| cmp\_cnt | 5 | 1 CLK\_SLOW\_SC | 5’b0 | It is used to record the number of data compared. |
| DEGL\_TIME | 1 | 1 CLK\_SLOW\_SC | 1’b0 | When all the data comparing ends, the DEGL\_TIME pulse (1 clock period) is generated. When the DEGL\_TIME = 1, the deglitch module is enabled. |
| UPDATED | 1 | 1 CLK\_SLOW\_SC | 1’b0 | When the falling edge of CMP\_UNDERWAY is detected, the UPDATED = 1. It is used to enable the road from comparator result to the result register in top module. |

### OVUV\_OTUT\_CMP Function Descriptions

The OVUV\_OTUT\_CMP module has the following functions:

• Latch OVUV\_OTUT\_EN\_REG, CELL\_OV\_THRESH\_REG, CELL\_UV\_THRESH\_REG, GPIO\_OTUT\_THRESH\_SEL\_REG, GPIO\_OT\_PACK\_THRESH\_REG, GPIO\_OT\_PCB\_THRESH\_REG, GPIO\_UT\_PACK\_THRESH\_REG, GPIO\_UT\_PCB\_THRESH\_REG, CB\_OT\_PACK\_THRESH\_REG, CB\_OT\_PCB\_THRESH\_REG, OVUV\_DEGL\_REG to OVUV\_OTUT\_EN, CELL\_OV\_THRESH, CELL\_UV\_THRESH, GPIO\_OTUT\_THRESH\_SEL, GPIO\_OT\_PACK\_THRESH, GPIO\_OT\_PCB\_THRESH, GPIO\_UT\_PACK\_THRESH, GPIO\_UT\_PCB\_THRESH, CB\_OT\_PACK\_THRESH, CB\_OT\_PCB\_THRESH, OVUV\_DEGL once MON\_WAKE\_GO or ADC\_GO\_DLY is high; (Func 1) (HWR001\_OVUV\_OTUT\_CMP)

• Compare ADC\_DATA\_LPF with CELL\_OV\_THRESH and CELL\_UV\_THRESH when RR\_END is high, and output CELL\_OVUV according to OVUV\_DEGL when OVUV\_OTUT\_EN is high; (Func 2) (HWR002\_OVUV\_OTUT\_CMP)

• Compare OTH\_ADC\_DATA with GPIO\_OT\_PACK\_THRESH, GPIO\_OT\_PCB\_THRESH, GPIO\_UT\_PACK\_THRESH, GPIO\_UT\_PCB\_THRESH, CB\_OT\_PACK\_THRESH, CB\_OT\_PCB\_THRESH according to GPIO\_OTUT\_THRESH\_SEL when RR\_END is high, and output GPIO\_OTUT, GPIO\_CBOT when OVUV\_OTUT\_EN is high; (Func 3) (HWR003\_OVUV\_OTUT\_CMP)

• Reset when OVUV\_OTUT\_EN is low; (Func 4) (HWR004\_OVUV\_OTUT\_CMP)

• Output CELL\_OVUV until counter=OVUV\_DEGL; (Func 5) (HWR005\_OVUV\_OTUT\_CMP)

• The counter will +1 when fault is detected; (Func 6) (HWR005\_OVUV\_OTUT\_CMP)

• The max of counter is OVUV\_DEGL; (Func 7) (HWR005\_OVUV\_OTUT\_CMP)

• The counter will -1 when fault is not detected; (Func 8) (HWR005\_OVUV\_OTUT\_CMP)

• Update TWARN\_THRESH\_REG into TWARN\_THRESH when ADC\_GO\_DLY or MON\_WAKE\_GO is high; (Func 9) (HWSR1\_OVUV\_OTUT\_CMP)

• Compare the gap between OTH\_ADC\_DATA with TWARN\_THRESH when RR\_END is high; (Once over range, output TWARN) (Func 10) (HWSR2\_OVUV\_OTUT\_CMP)

• TWARN TWARN\_THRESH covers from 110℃ to 145℃, 5℃ step; (Func 11) (HWSR2\_OVUV\_OTUT\_CMP)

• OVUV\_OTUT\_EN is ignored when TWARN comparison. (Func 12) (HWSR3\_OVUV\_OTUT\_CMP)

Above functions can be found in the following timing diagrams. Among them, Fig 2 is about data loading from registers, Fig 3 is about “UV” and “OT”, Fig 4 is about “OV” and “UT”, Fig 5 is about “CBOT” and “TWARN”.

Func 1 & Func 9: Sample the value of OVUV\_OTUT\_CMP\_START (its generation can be found in Fig 1) using CLK\_SLOW\_SC. When the high level of OVUV\_OTUT\_CMP\_START is detected, the value of OVUV\_OTUT\_EN, CELL\_OV\_THRESH, CELL\_UV\_THRESH, GPIO\_OTUT\_THRESH\_SEL, GPIO\_OT\_PACK\_THRESH, GPIO\_OT\_PCB\_THRESH, GPIO\_UT\_PACK\_THRESH, GPIO\_UT\_PCB\_THRESH, CB\_OT\_PACK\_THRESH, CB\_OT\_PCB\_THRESH, OVUV\_DEGL will be set to the value of corresponding registers.

Func 2 & Func 3 & Func 10: Complement it using TDM (Time Division Multiplexer) method. When the posedge of RR\_END is detected, CMP\_UNDERWAY is set to 1 and the counter starts to count. When the counter value is 31, the CMP\_UNDERWAY and the counter is cleared at the next clock posedge. The different counter values are corresponding to different channels. If deglitch is needed, the deglitch will be accomplished when counter value = 20.

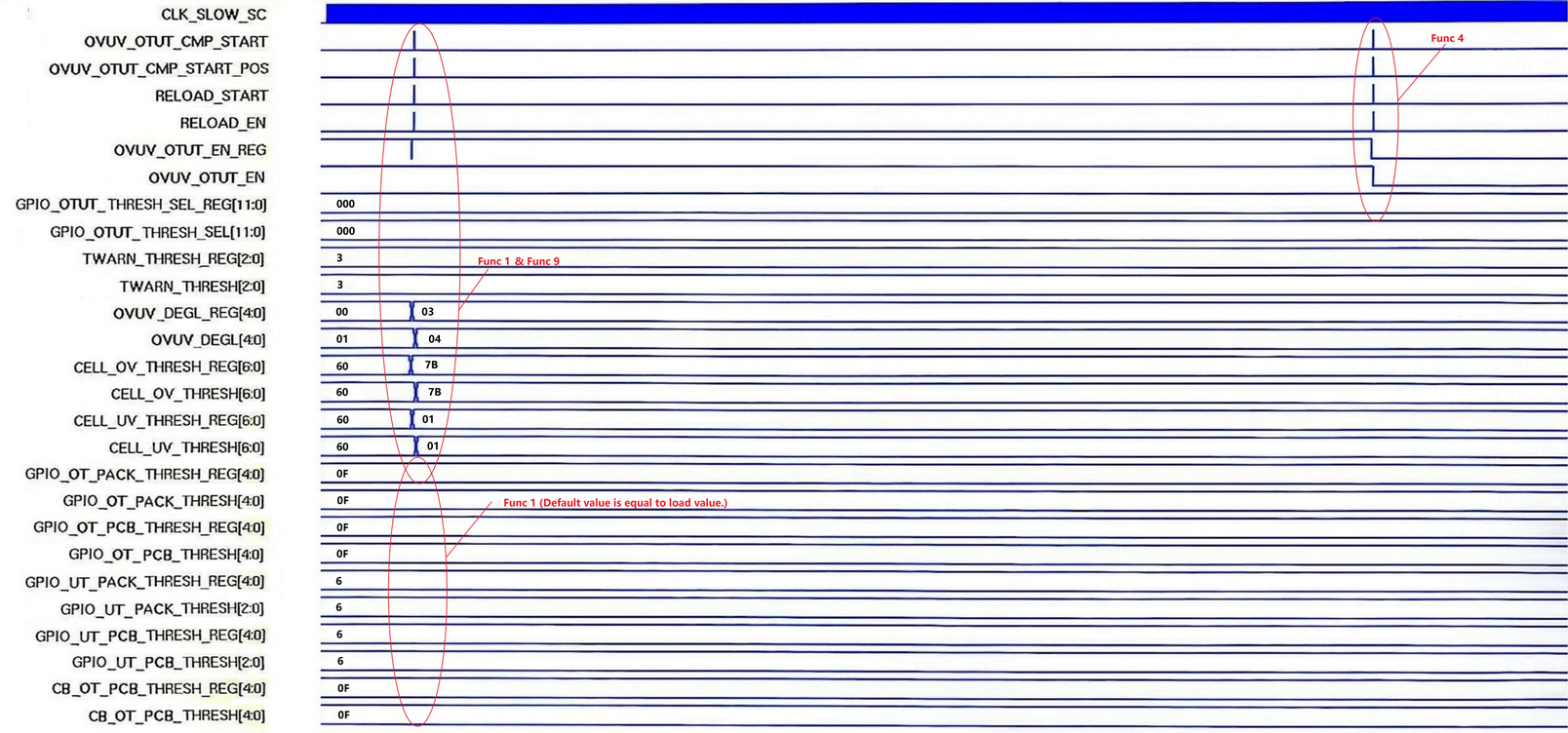


Fig 2. OVUV\_OTUT\_CMP Timing Diagram 1

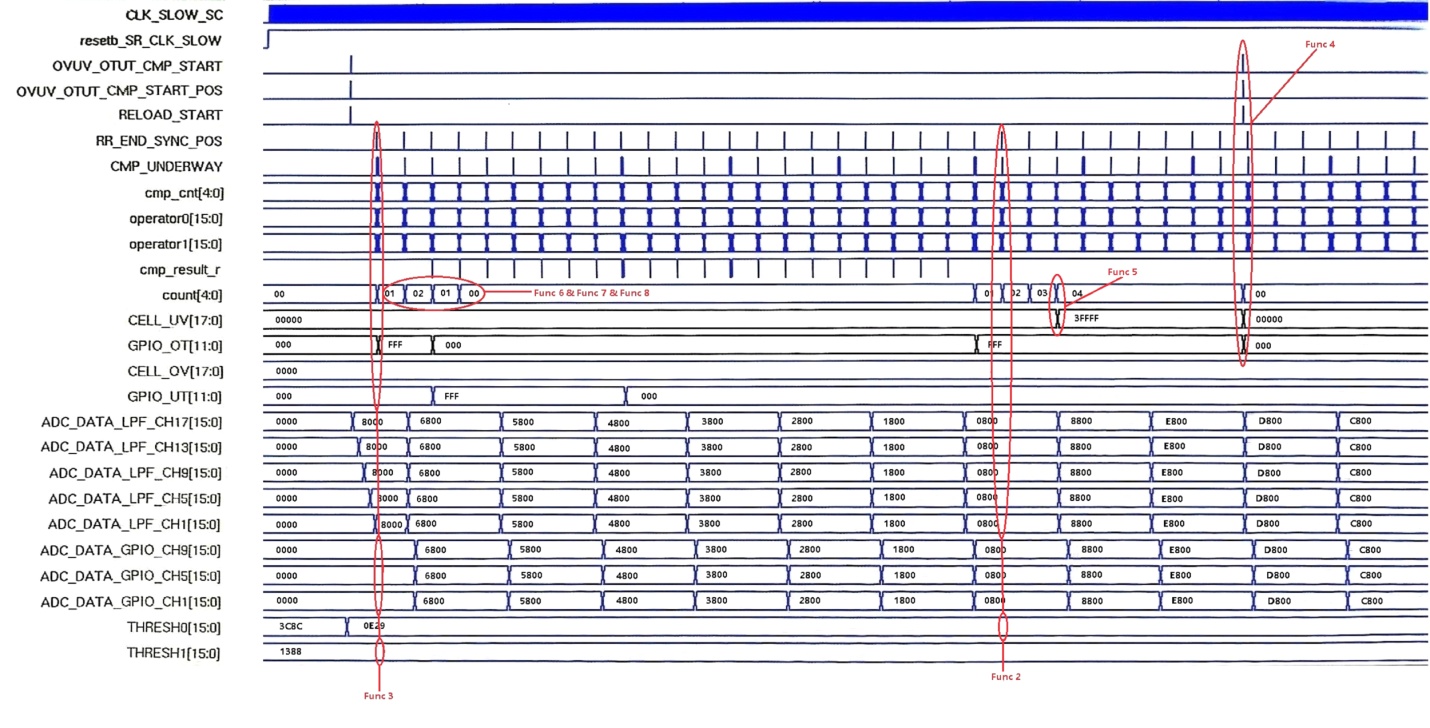


Fig 3. OVUV\_OTUT\_CMP Timing Diagram 2

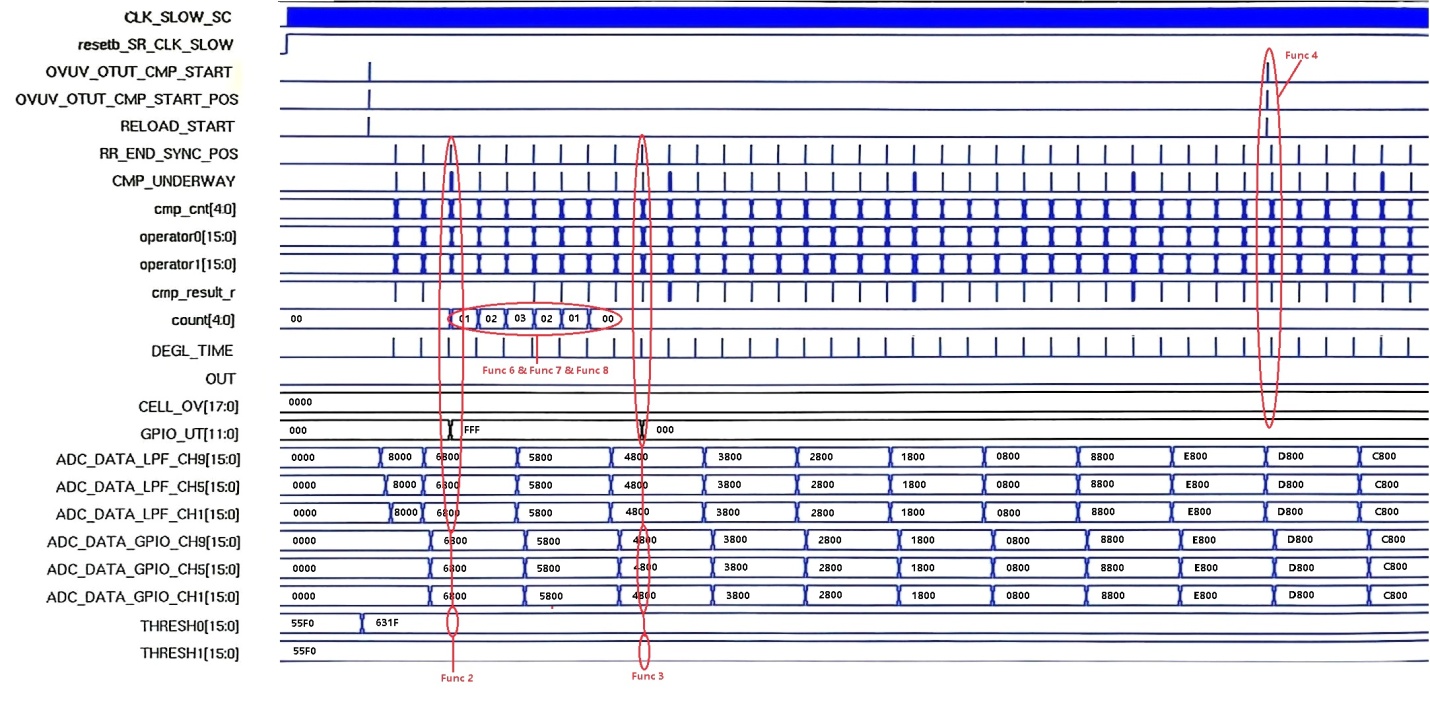


Fig 4. OVUV\_OTUT\_CMP Timing Diagram 3

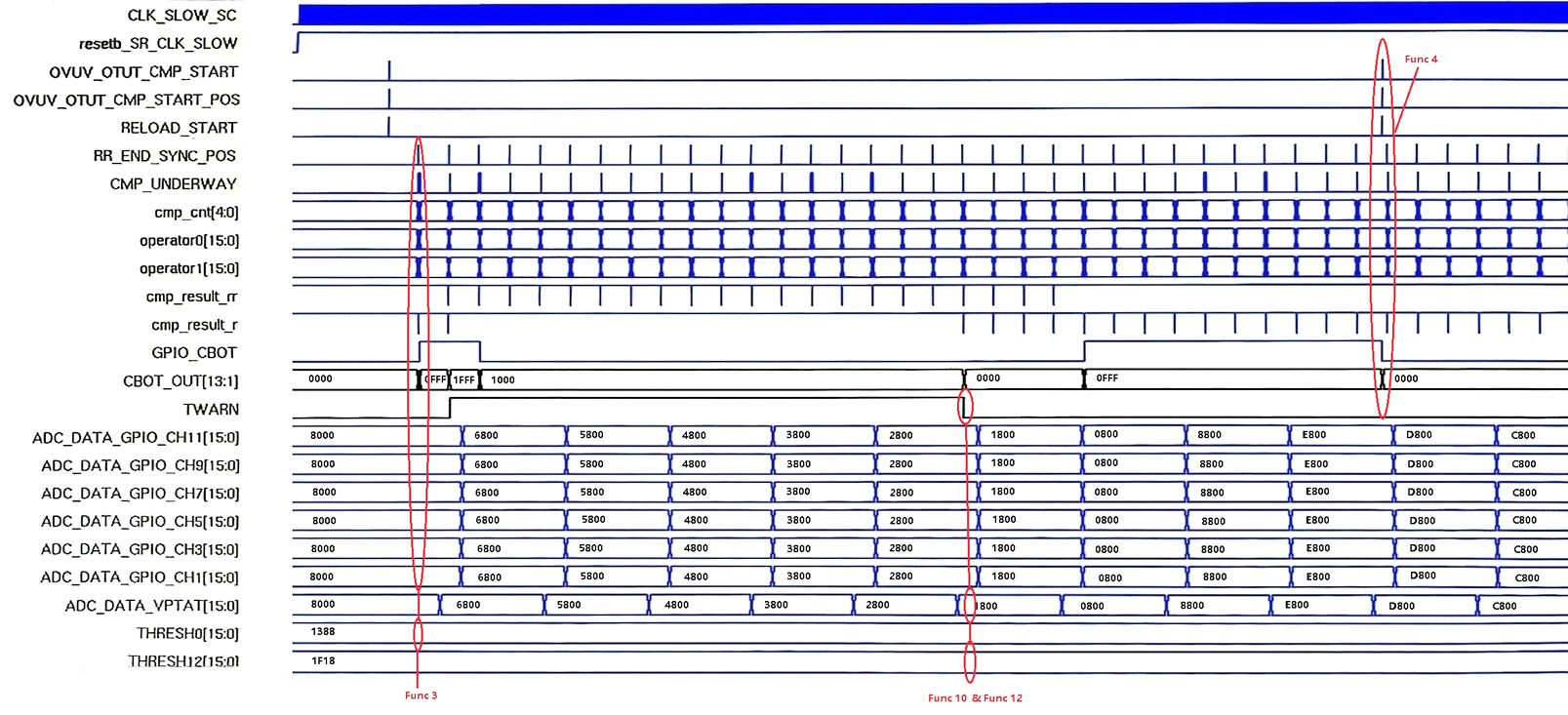


Fig 5. OVUV\_OTUT\_CMP Timing Diagram 4